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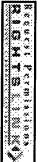
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Flash memory BIOS for PC and notebook computers

Intel Corp., Folsom, CA, USA

This paper appears in: Communications, Computers and Signal Processing, 1991., IEEE Pacific Rim Conference on

Publication Date: 9-10 May 1991

On page(s): 692 - 695 vol.2 Meeting Date: 05/09/1991 - 05/10/1991

Location: Victoria, BC

INSPEC Accession Number: 4208870

Digital Object Identifier: 10.1109/PACRIM.1991.160834

Posted online: 2002-08-06 17:47:24.0

controller is an ideal storage medium for PC and notebook computer BIOS code internal program and erase sequence controller. A 1-Mb block erasable flash memory with an internal program and erase sequence providing boot and recovery code protected from inadvertent program or erasure. BIOS code is easily updated in flash memory containing an memory with update software provided on a desk or by modem. Block erasable flash memory provides the capability of BIOS updates while BIOS storage does not require EEPROM's feature of byte erasure. Rapid and inexpensive BIOS revisions can be accomplished in flash bulk erasable flash memory, or block erasable flash memory. Updating BIOS stored in ROM or EPROM requires much time and money increasing computer complexity requires rapid and convenient BIOS modifications. BIOS code can be stored in ROM, EPROM, EEPROM, The author describes a flash memory device used to store the basic input/output system (BIOS) of a PC or notebook computer. Rapidly

index Terms

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digital storage input-output programs microcomputers

Non-controlled Indexing

memory boot code bulk erasable flash memory erase sequence controller flash memory device internal 1 MB BIOS code BIOS undates EEPROM EPROM PC ROM basic input/butput system black erasable flash

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Author Keywords

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<u>L5</u>	(firmware near5 memory) same (flag or pointer)	237	<u>L5</u>
<u>L4</u>	(LPC near5 memory) same (flag or pointer)	16	<u>L4</u>
<u>L3</u>	(LPC near5 memory) same (firmware near5 memory) same (flag or pointer)	1	<u>L3</u>
DB=EB	PAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
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Terms	Documents
(LPC near5 memory) and (firmware near5 memory)	0

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<u>L9</u>	((LPC near5 memory) same (flag or pointer)) and((firmware near5 memory) same (flag or pointer))	1	<u>L9</u>
<u>L8</u>	17 and firmware	2	<u>L8</u>
<u>L7</u>	14 or L6	18	<u>L7</u>
<u>L6</u>	("low pin count" near5 memory) same (flag or pointer)	3	<u>L6</u>
<u>L5</u>	(firmware near5 memory) same (flag or pointer)	237	<u>L5</u>
<u>L4</u>	(LPC near5 memory) same (flag or pointer)	16	<u>L4</u>
<u>L3</u>	(LPC near5 memory) same (firmware near5 memory) same (flag or pointer)	1	<u>L3</u>
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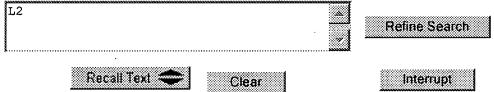
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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
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<u>L1</u> (("low pin count" or LPC) near5 memory) and ((firmware or BIOS) near5 memory)	44	L1

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Terms	Documents
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Terms	Documents
(LPC adj1 memory) same (firmware adj1 memory) same (flag or pointer)	0

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L2 (LPC adj1 memory) same (firmware adj1 memory) same (flag or pointer) 0	<u>L2</u>
DB=PGPB, $USPT$, $USOC$; $PLUR=YES$; $OP=OR$		
L1 (LPC adj1 memory) same (firmware adj1 memory) same (flag or pointer) 1	<u>L1</u>